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REMARKS

The Examiner is thanked for the allowance of Claim 24. Applicant has added dependent Claims 28-37 to such allowed independent claim. Since such dependent claims depend on the allowed Claim 24, applicant emphasizes that such claim amendment would not require an additional search and/or consideration.

The Examiner has requested that the related application section be updated. Applicant has amended the specification hereinabove, per the Examiner's request.

The Examiner has again rejected Claims 1-9, 11-13, and 15-23 under 35 U.S.C. 103(a) as being unpatentable over Novak et al. (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler et al. (US Patent No. 6,622,225, hereinafter "Kessler"). Applicant again respectfully disagrees with such rejection.

Specifically, the Examiner continues to rely on the following excerpt from Kessler to make a prior art showing of applicant's claimed "wherein the memory controller is capable of restoring the activate commands to a row and a bank associated with the read or write commands at a head of a read or write queue" (see all independent claims, except Claims 24-25).

"A computer system includes a memory controller interfacing the processor to a memory system. The memory controller supports a memory system with a plurality of memory devices, with multiple memory banks in each memory device. The memory controller supports simultaneous memory accesses to different memory banks. Memory bank conflicts are avoided by examining each transaction before it is loaded in the memory transaction queue. On a first clock cycle, the new pending memory request is transferred from a pending request queue to a memory mapper. On the subsequent clock cycle, the memory mapper formats the pending memory request into separate signals identifying the DEVICE, BANK, ROW and COLUMN to be accessed by the pending transaction. In the next clock cycle, the DEVICE and BANK signals are compared with every entry in the memory transaction queue to determine if a bank conflict exists. If so, the new memory request is rejected and recycled to the pending request queue." (see Abstract)

In response to applicant's previous arguments, the Examiner now notes

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applicant's use of "capable of being" language in the context of the above claim language. Specifically, the Examiner stated that such language does not claim an act or a structure that actually restores. Applicant respectfully disagrees. Nevertheless, in the spirit of expediting the prosecution of the present application, applicant has clarified the claims to address this newly-presented issue. Since the Examiner has presented such issue under final, applicant emphasizes that such claim amendment would not require an additional search and/or consideration.

The Examiner continues by arguing that Novak "has the capability to actually issue activate commands to a row and a bank associated with the read or write commands and the same structure is capable of supporting restoration of an activate command." Moreover, the Examiner continues by arguing that "[a]n activate command to a row and a bank is brought back into existence along with other appropriate primitive commands (i.e. precharge, read/write) when a recycled memory request gets decoded again in an attempt to access the memory again."

Applicant respectfully disagrees with these assertions. First, earlier in the present office action, the Examiner states that "[n]or does Novak disclose that the activate commands are capable of being restored to a row and a bank associated with the read or write command at a head of the associated read or write queue," and the Examiner states that he is relying on Kessler to meet such limitation. Thus, it appears that the Examiner is making conflicting statements, namely admitting that Novak does not disclose the claim limitations at issue, and then asserting that they are met by Novak.

Further, the Examiner's assertions are baseless, as no excerpts have been cited. Still yet, the Examiner's statements are simply incorrect. For example, the Examiner states that Novak "is capable of supporting restoration of an activate command." After carefully reviewing the entire Novak reference, this is simply incorrect.

Still yet, the Examiner continues to support his position by stating that applicant's claim limitations are met "when a recycled memory request gets decoded

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again in an attempt to access the memory again." Again, after carefully reviewing the entire Novak reference, there is absolutely no mention of "recycling" any memory request. Further, even if there were such a suggestion, it would be improper to leap to the conclusion that Novak even suggests applicant's claimed "restoring the activate commands to a row and a bank associated with the read or write commands at a head of a read or write queue."

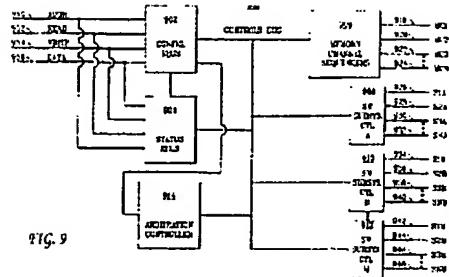
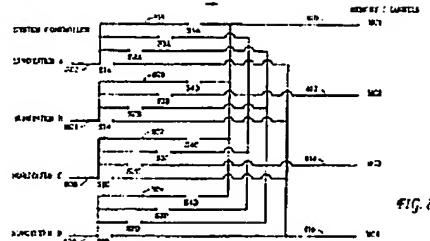
Since no specific prior art showing has been made, it appears that the Examiner is relying on an inherency argument regarding the above emphasized claim limitations. In view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested. (See MPEP 2112)

Applicant respectfully maintains that the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to at least suggest all of applicant's claim limitations. Again, a notice of allowance or a specific prior art showing of each of the foregoing limitations, in combination with the remaining claim elements is respectfully requested.

The Examiner has again rejected Claim 25 under 35 U.S.C. 102(e) as being anticipated by Margulis (US Patent No. 6,057,862, hereinafter "Margulis"). Applicant respectfully disagrees with such rejection.

Specifically, the Examiner has modified the excerpts he relies upon to reject such claim. In particular, the Examiner now relies on the following excerpts from Margulis to meet applicant's claimed "at least three memory controller subsystems".

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Specifically, the Examiner points to items 802-808 and 908-912 to meet applicant's claimed "at least three memory controller subsystems." First, items 802-808 are mere "subsystems" (i.e. display, CPU, etc.) per the specification of Margulis. Further, items 908-912 in no way meet applicant's claimed "wherein a first one of the memory controller subsystems is coupled only to a graphics unit computer component, a second one of the memory controller subsystems is coupled only to a central processing computer component, and a third one of the memory controller subsystems is coupled only to a display refresh module computer component" (emphasis added).

It is clear from both Fig. 8 and Fig. 9 that any components therein which may allegedly be considered "at least three memory controller subsystems" are coupled to all of the computer components, and thus do not meet a first one of the memory controller subsystems coupled only to a graphics unit computer component, a second one of the memory controller subsystems coupled only to a central processing computer component, and a third one of the memory controller subsystems coupled only to a display refresh module computer component, as claimed.

Only applicant teaches and claims that each memory subsystem is coupled only to one computer component. A notice of allowance or a specific prior art showing of each of the foregoing limitations, in combination with the remaining claim elements is respectfully requested.

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Applicant further notes that the Examiner's application of the prior art to each of applicant's dependent claims is further replete with deficiencies. Just by way of example, the Examiner relies on the following excerpt from Novak to meet applicant's claimed "wherein the restoring utilizes a field in the read or write queue that contains an activate write address" (see Claim 26).

RWQ Fields	
Field	Description
V	V valid RWQ entry. Possibly cleared by a RxD status
Trd_Cn[2:0]	Trd is initialized to Config_Trd whenever an entry with AQ field set enters the oldest entry RWQ[0]. This field is initialized with 1's corresponding to the number of cycles the transaction must wait. Every cycle that Aquip is cleared this field is right shifted and the entry cannot be placed onto the SDRAM bus until Trd_Cn[0]=0. Ensures that read/write operations that require an activate issue after the activate completes
PQ_dsp	Prevents RWQ entry item issuing until corresponding PQ entry issues
Aquip	Activate Queue dependency. This field is set by the SMC_AQ signal for PMic and PNB_MRA requests and cleared whenever an Activate transaction is returned by the AQ_Accept signal, i.e. accepted by the SPM
PMic	When an entry with this field enters the bottom of the RWQ it signals the PQ that it can now proceed and then this field must be cleared. This field used to synchronize PQ and RWQ. Also ensures of read/write latency to new 4 S'c by adding 1 extra cycle of latency.
Prc	When an entry with this field enters the bottom of the RWQ it signals the PQ that it can now proceed and then this entry gets shifted out on the next cycle since it only serves as a placeholder in the RWQ and does not represent a valid Read or Write
BL[2:0]	Burst length: 000=1QW; 001=2QW; 010=4QW; 100=8QW; 101=16QW; 110=32QW; 111=64QW Set by NXTReq_BL[2:0]
CS[7:0]	Determines CS that transaction requires Set by NXTReq_CS[7:0]
Col[14:0]	Determines Bank and Col that transaction requires Set by NXTReq_Col[14:0]
R	Read Write: 1=Read Set by NXTReq_R
ID[7:0]	See IGLD description for more details Set by NXTReq_ID[7:0]
ECC	ECC - SMC, ECC-NxTReq_PartialWr & Config_ECC* For reads this field tells the MDP to slice SDRAM data into ECC merge blocks. For writes this field tells the MDP to merge incoming write data with the ECC merge buffer according to incoming write data byte enables and then use this merged data on the SDRAM data bus

Fig. 7

First, Novak does not suggest any restoring of an activate command, and thus inherently can not meet the present claim limitations. Further, after carefully reviewing the above figure, it is clear that there is simply no restoring that specifically utilizes a field in the read or write queue that contains an activate write address. A notice of allowance or a specific prior art showing of each of the

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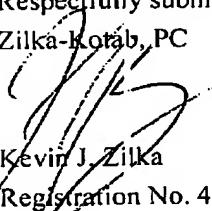
foregoing limitations, in combination with the remaining claim elements is respectfully requested.

All of the independent claims are deemed allowable. Moreover, the remaining claims are also deemed allowable by virtue of their dependence from the independent claims. An allowance is respectfully requested.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. For payment of any fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP033A/P000873).

Respectfully submitted,

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